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Presented for filing is a new continuation patent application of:

Applicant: ERIC R. FOSSUM and ROBERT NIXON

Title: CMOS ACTIVE PIXEL SENSOR TYPE IMAGING SYSTEM ON A CHIP

Enclosed are the following papers, including all those required to receive a filing date under 37 CFR §1.53:

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Specification	44
Claims	37
Abstract	1
Declaration	2
Drawing(s)	10

"EXPRESS MAIL" Mailing Label Number EM 320 642 608 US
Date of Deposit 07/21/98
I hereby certify under 37 CFR 1.10 that this correspondence is being deposited with the United States Postal Service as **"Express Mail Post Office To Addressee"** with sufficient postage on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

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Enclosures:

- Rule 63 declaration, copy from a previous application under rule 63(d) for continuation or divisional only.

- Information Disclosure Statement: Applicant calls attention to documents listed on attached forms PTO-892 and PTO-1449 from parent case(s). Per Rule 97(d) copies of those documents are not provided.

- Postcard.

This application is a continuation and claims the benefit of priority under 35 USC §120 of U.S. application serial no. 08/188,032, filed 1/28/94, and serial no. 08/789,608, filed 1/24/97; and also claims the benefit of priority under 35 USC §119(e)(1) of U.S. provisional application serial no. 60/010,678, filed 1/26/96 . The disclosure of the prior applications is considered part of (and is incorporated by reference in) the disclosure of this application.

<u>Preliminary Amendment</u>:

Page 1 of the specification, before line 1, insert --This is a continuation of U.S. application serial no. 08/188,032, filed 1/28/94; provisional application serial no. 60/010,678, filed 1/26/96; and, serial no. 08/789,608, filed 1/24/97 (pending).--

The prior application is assigned of record to California Institute of Technology, a non-profit corporation of California, by virtue of an assignment submitted to the Patent and Trademark Office for recording on May 19, 1997, at Reel 8508/Frame 0325.

This application is entitled to small entity status. Small entity status established in a previous application is still proper.

Basic filing fee	$ 395.00
Total claims in excess of 20 times $11.00	1320.00
Independent claims in excess of 3 times $41.00	451.00
Multiple dependent claims	0.00
Total filing fee:	$ 2166.00

A check for the filing fee is enclosed. Please apply any other required fees or any credits to deposit account 06-1050, referencing the attorney docket number shown above.

If this application is found to be INCOMPLETE, or if a telephone conference would otherwise be helpful, please call the undersigned at 619/678-5070.

Kindly acknowledge receipt of this application by returning the enclosed postcard.

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Respectfully submitted,

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Enclosures

63768.LJ1

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: CMOS ACTIVE PIXEL SENSOR TYPE IMAGING SYSTEM ON A CHIP

APPLICANT: ERIC R. FOSSUM and ROBERT NIXON

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CMOS ACTIVE PIXEL SENSOR TYPE IMAGING SYSTEM ON A CHIP

This is a continuation-in-part of U.S. Application Serial No. 08/188,032, filed January 28, 1994, and claims priority from provisional application no 60/010,678 having a filing date of January 26, 1996.

Origin

The invention described herein was made in performance of work under NASA contract and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the contractor has elected to retain title.

Field of the Invention

The present invention relates to a single chip imaging sensor.

Background and Summary of the Invention

Imaging technology is the science of converting an image to a signal indicative thereof. Imaging systems have

broad applications in many fields, including commercial, consumer, industrial, medical, defense and scientific markets.

The original image sensors included an array of photosensitive elements in series with switching elements. Each photosensitive element received an image of a portion of the scene being imaged. That portion is called a picture element or pixel. The image obtaining elements produce an electrical signal indicative of the image plus a noise component. Various techniques have been used in the art to minimize the noise, to thereby produce an output signal that closely follows the image.

Size minimization is also important. The development of the solid state charge coupled device ("CCD")

in the early 1970's led to more compact image systems. CCDs use a process of repeated lateral transfer of charge in an MOS electrode-based analog shift register. Photo-generated signal electrons are read after they are shifted into appropriate positions. However, the shifting process requires high fidelity and low loss. A specialized semiconductor fabrication process was used to obtain these characteristics.

CCDs are mostly capacitive devices and hence dissipate very little power. The major power dissipation in a CCD system is from the support electronics. One reason for this problem is because of the realities of forming a CCD system.

The specialized semiconductor fabrication process alluded to above is not generally CMOS compatible. Hence, the support circuitry for such a CCD has been formed using control electronics which were not generally CMOS compatible. The control electronics have dissipated an inordinate percentage of the power in such imaging devices. For example, CCD-based camcorder imaging systems typically operate for an hour on an 1800 mA-hr 6 V NiCad rechargeable battery, corresponding to 10.8 W of power consumption. Approximately 8 watts of this is dissipated in the imaging system. The rest is used by the tape recording system, display, and autofocus servos.

Space-based imaging systems often have similar problems. The space based systems operate at lower pixel

rates, but with a lower degree of integration, and typically dissipate 20 watts or more.

The CCD has many characteristics which cause it to act like a chip-sized MOS capacitor. The large capacitance of the MOS device, for example, requires large clock swings, ΔV, of the order of 5-15 V to achieve high charge transfer efficiency. The clock drive electronics dissipation is proportional to $C\Delta V^2 f$, and hence becomes large. In addition, the need for various CCD clocking voltages (e.g. 7 or more different voltage levels) leads to numerous power supplies with their attendant inefficiencies in conversion.

Signal chain electronics that perform correlated double sampling ("CDS") for noise reduction and

amplification, and especially analog to digital converters (ADC), also dissipate significant power.

The inventors also noted other inefficiencies in imaging systems. These inefficiencies included fill factor inefficiencies, fixed pattern noise, clock pick up, temporal noise and large pixel size.

Active pixel sensors, such as described in U.S. Patent no. 5,471,515, the disclosure of which is incorporated by reference herein, use special techniques to integrate both the photodetector and the readout amplifier into the pixel area or adjacent the pixel area. This allows the signal indicative of the pixel to be read out directly. These techniques have enabled use of a logic family whose fabrication processes are compatible with CMOS. This has

enabled the controlling circuitry to be made from CMOS or some other low power-dissipating logic family.

The inventors of the present invention have recognized techniques and special efficiencies that are obtained by specialized support electronics that are integrated onto the same substrate as the photosensitive element. Aspects of the present invention include integration, timing, control electronics, signal chain electronics, A/D conversion, and other important control systems integrated on the same substrate as the photosensitive element.

It is hence an object of the present invention to provide for the integration of an entire imaging system on a chip.

Brief Description of the Drawings

Figure 1 shows a basic block diagram of a CMOS active pixel circuit;

Figure 2 shows a graph of typical APS quantum efficiency;

Figure 3 shows the block diagram of the overall chip including drivers and controlling structures;

Figures 4A and 4B show the timing diagrams for photogate operation and photodiode operation, respectively;

Figure 5 shows a schematic of the active pixel sensor unit cell and readout circuitry;

Figure 6 shows a timing diagram for setup and readout;

Figure 7 shows a drawing of an actual layout of the pixel and control circuitry;

Figure 8 shows a block diagram of a CMOS APS chip; and

Figure 9 shows an exemplary pixel layout.

<u>Description of the Preferred Embodiments</u>

An active pixel sensor is herewith described with reference to Figures 1-4.

A block diagram of a CMOS active pixel circuit is shown in Fig. 1. The device has a pixel circuit 150, and a column circuit 155.

Incident photons pass through the photogate ("PG") 100 in the pixel circuit 150 and generate electrons which

are integrated and stored under PG 100. A number of the pixel circuits are arranged in each row of the circuit. One of the rows is selected for readout by enabling the row selection transistor 102 ("RS").

In the preferred embodiment, the floating diffusion output node 104 ("FD") is first reset by pulsing reset transistor ("RST") 106. The resultant voltage on FD 104 is read out from the pixel circuitry onto the column bus 112 using the source follower 110 within the pixel. The voltage on the column bus 112 is sampled onto a first holding capacitor 114 by pulsing transistor SHR 116. This initial charge is used as the baseline.

The signal charge is then transferred to FD 104 by pulsing PG 100 low. The voltage on FD 104 drops in

proportion to the number of photoelectrons and the capacitance of FD. The new voltage on the column bus 112 is sampled onto a second capacitor 118 by pulsing SHR 120. The difference between the voltages on first capacitor 114 and second capacitor 118 is therefore indicative of the number of photoelectrons that were allowed to enter the floating diffusion.

The capacitors 114, 118 are preferably 1-4 pf capacitors.

All pixels on a selected row are processed simultaneously and sampled onto capacitor at the bottom of their respective columns. The column-parallel sampling process typically takes 1-10 μsec, and preferably occurs

during the so-called horizontal blanking interval of a video image.

Each column is successively selected for read-out by turning on column selection p-channel transistors ("CS") 130. The p-channel source-followers 122, 124 in the column respectively drive the signal (SIG) and horizontal reset (RST) bus lines. These lines are loaded by p-channel load transistors which can be sent directly to a pad for off-chip drive, or can be buffered.

Noise in the sensor is preferably suppressed by the above-described correlated double sampling ("CDS") between the pixel output just after reset, before and after signal charge transfer to FD as described above. The CDS suppresses kTC noise from pixel reset, suppresses 1/f noise

from the in-pixel source follower, and suppresses fixed pattern noise (FPN) originating from pixel-to-pixel variation in source follower threshold voltage.

The inventors found, however, that kTC noise may be reintroduced by sampling the signal onto the capacitors 114, 118 at the bottom of the column. Typical output noise measured in CMOS APS arrays is of the order of 140-170 μV/e-, corresponding to noise of the order of 13-25 electrons r.m.s. This is similar to noise obtained in most commercial CCDs, through scientific CCDs have been reported with read noise in the 3-5 electrons rms.

Typical biasing for each column's source-follower is 10 μA. This permits charging of the sampling capacitors in

the allotted time. The source-followers can then be turned off by cutting the voltage on each load transistor.

The sampling average power dissipation P_s corresponds to :

$$P_s = n\ I\ V\ d$$

where n is number of columns, I is the load transistor bias, V is the supply voltage, and d is the duty cycle. Using n=512, I=μA, V=5V and d=10%, a value for Ps of 2.5mW is obtained.

A load current of 1 mA or more is needed to drive the horizontal bus lines at the video scan rate. The power dissipated is typically 5 mW.

Quantum efficiency measured in this CMOS APS array is similar to that for interline CCDs. A typical response curve is shown in Fig. 2. The inventors noticed from this that the quantum efficiency reflects significant responsivity in the "dead" part of the pixel; the part containing the readout circuitry rather than the photogate collector. The responsiveness was measured by intra-pixel laser spot scanning.

The inventors postulate the following reason. The transistor gate and channel absorb photons with short absorption lengths (i.e. blue/green). However, longer wavelength photons penetrate through these regions. The subsequently-generated carriers diffuse laterally and are subsequently collected by the photogate.

Thus, despite a fill factor of 25%-30%, the CMOS APS achieves quantum efficiencies that peak between 30%-35% in the red and near infrared. Microlenses are preferably added to refract photoelectrons from the dead part to a live part and hence improve quantum efficiency.

An important feature of the system described herein is the integration of on-chip timing and control circuits within the same substrate that houses the pixel array and the signal chain electronics. A block diagram of the chip architecture is shown in Fig. 3.

The analog outputs VS_out (signal) and VR_out (reset) are as described above. The digital outputs include FRAME and READ. Most of the inputs to the chip are asynchronous digital signals, as described herein.

The chip includes a pixel array 300, which is driven by on-chip electronics. Timing and control circuit 302 drives row electronics 310, and column electronics 320.

The control circuits can command read-out of any area of interest within the array. Row decoder 312 controls row drivers 314 which can select a certain row for readout. A specific row is selected by entry of a row value 316 which is output from timing and control 302. Row value 316 is stored in latch 318 which drives counter 319. Counter 319 can allow selection of subsequent rows that follow the current row. Similarly, columns can be selected and accessed by latches 322, counter 324, decoder 326 and column signal conditioning 328.

Each of the decoder counters can be preset to start and stop at any value that has been loaded into the chip via the 8-bit data bus 330. Therefore, as described above, selection of a row commands pixels in that row to be transferred to the appropriate row decoding elements, e.g., capacitors. Preferably there is one capacitor associated with each column. This provides for the sequential readout of rows using the column. The capacitors are preferably included within the column signal conditioner 328. Column decoders 326 also allow selection of only a certain column to be read. There are two parts of each column selection: where to start reading, and where to stop reading. Preferably the operation is carried out using counters and registers. A binary up-counter within the decoder 326 is

preset to the start value. A preset number of rows is used by loading the 2's compliment. The up counter then counts up until an overflow.

An alternate loading command is provided using the DEFAULT LOAD input line 332. Activation of this line forces all counters to a readout window of 128 x 128.

A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-bit latch via the input data bus 330. A 32-bit counter operates from one-fourth the clock input frequency and is preset at each frame from the latch. The counter can hence provide vary large integration delays. The input clock can be any frequency up to about 10 MHZ. The pixel readout rate is

tied to one-fourth the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration time. The integration time is therefore equal to the delay time and the readout time for a 2.5 MHZ clock. The maximum delay time is 2^{32} / 2.5 MHZ, or around 28 minutes. These values therefore easily allow obtaining a 30 Hz frame.

The timing and control circuit controls the phase generation to generate the sequences for accessing the rows. The sequences must occur in a specified order. However, different sequences are used for different modes of operation. The system is selectable between the photodiode mode of operation and the photogate mode of operation. The timing diagrams for the two gates are respectively shown in

Figures 4a and 4b. Figure 4a shows an operation to operate in the photogate mode and Figure 4b shows operating in the photodiode mode. These different timing diagrams show that different column operations are possible. Conceptually this is done as follows. Column fixed pattern noise is based on differences in source follower thresholds between the different transistors. For example, if the base bias on a transistor is V1, the output is V1 plus the threshold.

The column signal conditioning circuitry contains a double-delta sampling fixed pattern noise ("FPN") suppression stage that reduces FPN to below 0.2% sat with a random distribution. Since the APS is formed of a logic family that is compatible with CMOS, e.g., NMOS, the circuitry can be formed of CMOS. This allows power

dissipation in the timing and control digital circuitry to be minimized and to scale with clock rate.

An active pixel sensor includes both a photodetector and the readout amplifier integrated within the same substrate as the light collecting device, e.g., the photodiode. The readout amplifier is preferably within and/or associated with a pixel.

A first embodiment of the present invention is a 128 x 128 CMOS photodiode type active pixel sensor that includes on chip timing, control and signal train electronics. A more detailed drawing of the chip is shown in Figure 5. Asynchronous digital signals are converted by this chip to VS and VR analog outputs which are used to run the chip.

Pixel portion 500 includes a photodiode 502 which stores incident photons under photogate 504. The photons are integrated as electrons within the photogate well. The output is buffered by follower 508.

The rows are arranged into an array. A particular row is selected by the row transistor 514. This allows the information from within the selected pixel 500 to be passed to the column decoder circuitry. Reset transistor 530 is connected to a sink 532. Reset transistor is biased to a low potential level to allow all charge to bleed to sink 532, and hence hold the stored charge in reset. The system is removed from reset by biasing the gate to a level as shown. This level is less than a highest possible potential to thereby allow charge which accumulates above that level

to pass to sink 532. Hence, the charge cannot overflow in an undesired way. This suppresses the blooming effect.

The depicted photogate system is driven according to the readout sequence shown in Figure 6. A row is selected by activating row selecting transistor 514. The cycle begins by sampling the signal present on each column pixel in that row. Sampling is initiated by biasing transistor 526 to place the signal from each column pixel in the row onto the holding capacitor 510.

After the current pixel value has been transferred to the capacitor 510, the pixel in the row is reset by biasing reset transistor to a low level, to photodiode 502 to the preset voltage sink 532.

Correlated double sampling is effected by sampling the reset value, as a reset level, onto the holding capacitor 512. This is done by activating the reset transistor 516.

The voltage value of the reset branch of the column circuit is given by

$$Vcol\_R \approx \beta\{\alpha[V_{pdr} - V_{tpix}] - V_{tcolr}\}$$

Where α is the gain of the pixel source follower 508, β is the gain of the column source follower 526, and V_{pdr} is the voltage on the photodiode after reset, V_{tpix} is the threshold voltage of the pixel source follower and channel transistor, and V_{tcolr} is the threshold voltage of the column source follower p-channel transistor.

Using similar reasoning, the output voltage of the signal branch of the column circuit is

$$Vcol\_S \approx \beta\{\alpha[V_{pds} - V_{tpix}] - V_{tcols}\}$$

where V_{pds} is the voltage on the photodiode with the signal charge present and V_{tcols} is the threshold voltage of the column source-follower p-channel transistor.

The inventors have found experimentally that the peak-to-peak variation $V_{tcolr} - V_{tcols}$ is typically between 10 and 20 millivolts. This, however, is a source of column to column fixed pattern noise. The inventors herein suggest a double delta sampling technique to eliminate this column to column noise. The present approach represents an improved version of the previously-described double delta sampling circuitry. The operation proceeds as follows. A column is

first selected. After a settling time equivalent to half of the column selection period, a special double delta sampling technique is performed to remove the column fixed pattern noise. Therefore, the varying thresholds on the different transistors cause varying outputs. According to this aspect, the threshold outputs of these transistors are equalized using a capacitor to equalize the charge. The capacitor is applied with the charge before and after the voltage change. Therefore, the output of the capacitor represents the difference between before and after, and the fixed pattern noise component drops out of the equation.

This system uses a DDS switch 520 and first and second column select switches 522, 524 to short across the respective capacitors. All three switches are turned on to

short across the two sample and hold capacitors 510. This clamp operation is shown in line 8 of Figure 6.

Prior to the DDS operation, the reset and signal column components, Vcol_R and Vcol_S include their signal values plus a source follower voltage threshold component from the appropriate source follower. The object of the special following circuit of the present invention is to remove that source follower threshold component. The operation proceeds as follows. Prior to the beginning of some operation, the capacitors are precharged through clamp transistors to a clamp voltage V_{cl}. This is maintained by turning on clamp transistors 550 and 552 to connect the appropriate capacitors to the voltage V_{cl}. The clamp operation is shown on line 8 of Figure 6. Immediately after

the clamp is released, the DDS transistors 520, 522 and 524 are turned on. This has the effect of shorting across the capacitors 510 and 512. When the transistors are shorted, the voltage that is applied to the output drivers 554, 556 includes only the voltage threshold component. The differential amplification of the voltage render the output voltage free of the voltage threshold component. Mathematically, prior to clamp being deactivated, the output signals are:

$$VR\_OUT \simeq \gamma(V_{cl} - V_{tr})$$

and $$VS\_OUT \simeq \gamma(V_{cl} - V_{ts})$$

where γ is the gain of the third stage source-follower, V_{cl} is the clamp voltage, and V_{tr} and V_{ts} are the threshold voltages of the third stage source-follower n-channel

transistors, reset and signal branch respectively. Deactivation of the clamp circuit and simultaneous activation of the DDS switch causes several changes. The voltages in the two column branch sampling circuits equalize becoming:

$$V_{cs} = V_{cr} = \alpha[V_{pdr} - V_{tpix} + V_{pds} - V_{tpix}]/2$$

This in turn causes a change in Vcol_S and Vcol_R to:

$$Vcol\_R' \simeq \beta\{\alpha[V_{pdr} - V_{tpix} + V_{pds} - V_{tpix}]/2 - V_{tcolr}\}$$

and $$Vcol\_S' \simeq \beta\{\alpha[V_{pdr} - V_{tpix} + V_{pds} - V_{tpix}]/2 - V_{tcols}\}$$

Consequently, the voltage outputs change to:

$$VR\_OUT \simeq \gamma(V_{cl} - Vcol\_R' - Vcol\_R - V_{tr})$$

and $$VS\_OUT \simeq \gamma(V_{cl} - Vcol\_S' - Vcol\_S - V_{ts})$$

We note

$$Vcol\_S' - Vcol\_S = \beta\{\alpha[V_{pds} - V_{pdr}]/2\}$$

and $$Vcol\_R' - Vcol\_R = \beta\{\alpha[V_{pdr} - V_{pds}]/2\}$$

When the outputs are differentially amplified off-chip, the common clamp voltage Vcl is removed, leaving only the difference between signal and reset. The net differential output voltage is given by:

$$VR\_OUT - VS\_OUT = \alpha\beta\gamma(V_{pdr} - V_{pds} = V_{const})$$

Figure 7 shows the layout of the pixel for 128 x 128 array size device. This system formed a 19.2 micron pixel size using 1.2 μm n-well CMOS. The maximum clock rate is 10 MHZ, the maximum pixel rate is 2.5 MHZ and maximum integration delay is 1.6 x 10^9 clock periods.

A second embodiment uses similar design techniques to produce a 256 x 256 array size. This embodiment also uses a pixel with a photogate imaging element along with four transistors to perform the functions of readout, selection, and reset. Readout is preferably achieved using a column parallel architecture which is multiplexed one row at a time and then one column at a time through an on-chip amplifier/buffer. An important part of this embodiment, like the first embodiment, is the use of a chip common logic elements to control row and address decoders and delay counters.

This embodiment allows use in three modes of operation: Photogate mode, photodiode mode and differencing mode. The photogate mode is the standard mode for this

chip. The photodiode mode alters the readout timing to be similar to that for photodiode operation. The differencing mode alters the readout timing in such a way that the value of each pixel output is the difference between the current frame and the previous frame. The chip inputs that are required are a single +5 V power supply, start command, and parallel data load commands for defining integration time and windowing parameters. The output has two differential analog channels.

The second embodiment uses the block diagram of the chip architecture shown in figure 8. The analog outputs of VS_OUT (signal) and VR_OUT (reset), and digital outputs of FRAME and READ. The inputs to the chip are asynchronous digital signals. The chip includes addressing circuitry

allowing readout of any area of interest within the 256x256 array. The decoder includes counters that are preset to start and stop at any value that has been loaded into the chip via the 8-bit data bus. An alternate loading command is provided using the DEFAULT input line. Activation of this line forces all counters to a readout window of 256 x 256.

A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-bit latch via the input data bus. A 32-bit counter operates from one-fourth the clock input frequency and is preset at each frame from the latch. This counter allows forming very large integration delays. The input clock can be any frequency up

to about 10 MHZ. The pixel readout rate is tied to one fourth the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration time. A 30 HZ frame rate can be achieved without difficulty.

The chip is idle when the RUN command is deactivated. This is the recommended time for setting the operating parameters. However, these parameters can be set at any time because of the asynchronous nature of operation. When RUN is activated, the chip begins continuous readout of frames based on the parameters loaded in the control registers. When RUN is deactivated, the frame in progress runs to completion and then stops.

The 256x256 CMOS APS uses a system having a similar block diagram to those described previously. The pixel unit cell has a photogate (PG), a source-follower input transistor, a row selection transistor and a reset transistor. A load transistor VLN and two output branches to store the reset and signal levels are located at the bottom of each column of pixels. Each branch has a sample and hold capacitor (CS or CR) with a sampling switch (SHS or SHR) and a source-follower with a column-selection switch (COL). The reset and signal levels are read out differentially, allowing correlated double sampling to suppress 1/f noise and fixed pattern noise (not kTC noise) from the pixel.

A double delta sampling (DDS) circuit shorts the sampled signals during the readout cycle reducing column fixed pattern noise. These readout circuits are common to an entire column of pixels. The load transistors of the second set of source followers (VLP) and the subsequent clamp circuits and output source followers are common to the entire array. After a row has been selected, each pixel is reset (RESET) and the reset value is sampled (SHR) onto the holding capacitor CR. Next, the charge under each photogate in the row is transferred to the floating diffusion (FD). This is followed by sampling this level (SHS) onto holding capacitor CS. These signals are then placed on the output data bus by the column select circuitry. In the Photodiode mode this process, is reversed; first the charge under the

photogate is read out and then the reset level is sampled. This non-correlated double sampling mode would be primarily used with a photodiode, i.e., non active pixel sensor, pixel.

In the differencing mode, the capacitors CS and CR are used to store the signal from the previous frame and the current frame. This is achieved by altering the timing in the following way: Rather than starting with a reset operation, the signal on the floating diffusion is read out to one of the sample and hold capacitors. This represents the previous pixel value. The reset is then performed followed by a normal read operation. This value is then stored on the other sample and hold capacitor. The

difference between these two signals is now the frame to frame difference.

A simplified expression for the output of the reset branch of the column circuit is given by:

$$Vcol\_R \cong \beta\{\alpha[Vr - V_{tpix}] - V_{tcolr}\}$$

where α is the gain of the pixel source-follower, β is the gain of the column source-follower, Vr is the voltage on the floating diffusion after reset, V_{tpix} is the threshold voltage of the pixel source-follower n-channel transistor, and V_{tcolr} is the threshold voltage of the column source-follower p-channel transistor. Similarly, the output

voltage of the signal branch of the column circuit is given by:

$$Vcol\_S \cong \beta\{\alpha[V_S - V_{tpix}] - V_{tcols}\}$$

where V_S is the voltage on the floating diffusion with the signal charge present and V_{tcols} is the threshold voltage of the column source-follower p-channel transistor. Experimentally, the peak to peak variation in $V_{tcolr} - V_{tcols}$ is typically 10-20 mV. It is desirable to remove this source of column-to-column fixed pattern noise FPN. JPL has previously developed a double delta sampling (DDS) technique to eliminate the column-to-column FPN. This approach represented an improved version of the DDS circuitry.

Sequential readout of each column is as follows. First a column is selected. After a settling time equivalent to one-half the column selection period, the DDS is performed to remove column fixed pattern noise. In this operation, a DDS switch and two column selection switches on either side are used to short the two sample and hold capacitors CS and CR. Prior to the DDS operation the reset and signal outputs (Vcol_R and VCOL_S) contain their respective signal values plus a source follower voltage threshold component. The DDS switch is activated immediately after CLAMP is turned off. The result is a difference voltage coupled to the output drivers (VR_OUT and VS_OUT) that is free of the voltage threshold component.

This chip uses a similar pixel cell to that shown in Figure 5. Figure 9 shows the layout of the pixel cell. PG and RESET are routed horizontally in polysilicon while the pixel output is routed vertically in metal1. Metal2 was routed within the pixel for row selection. Metal2 was also used as a light shield and covers most of the active area outside of the pixel array. The designed fill factor of the pixel is approximately 21%.

According to another feature, a logo can be formed on the acquired image by using a light blocking metal light shield. The light shield is formed to cover certain pixels in the shape of the logo to be applied. This blocks out those underlying pixels in the array, thereby forming a logo in the shape of the blocked pixels.

The output saturation level of the sensor is 800mv when operated from a 5 V supply. Saturation is determined by the difference between the reset level on the floating diffusion node (e.g. 3 V) and the minimum voltage allowed on the pixel source follower gate (e.g. threshold voltage of approx. 0.8 volts). This corresponds to a full well of approximately 75,000 electrons. This can be increased by operating at a larger supply voltage, gaining about 47,000 e- per supply volt.

Dark current was measured at less than 500 pA/cm^2.

Conversion gain ($\mu V/e-$) was obtained per pixel by plotting the variance in pixel output as a function of mean signal for flat field exposure. The fixed pattern noise arising from dispersion in conversion gain was under 1% -

similar to the value found in CCDs and consistent with the well-controlled gain of a source-follower buffer.

The quantum efficiency of the detector was measured using a CVI 1/4 m monochromator and a tungsten/halogen light source, calibrated using a photodiode traceable to NIST standards.

What is claimed is:

1. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of active pixel type photoreceptors, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors.

2. A camera device as in claim 1 wherein said array of photoreceptors are controlled to output an entire row of said photoreceptors substantially simultaneously.

3. A camera device as in claim 1, further comprising double sampling charge storage elements on said substrate.

4. A camera device as in claim 3, wherein said timing circuit includes a timer for first sampling a reset level on a first of said charge storage elements, and then for second sampling a signal level on a second of said charge storage elements.

5. A camera device as in claim 2 further comprising a plurality of double sampling charge storage elements integrated on said substrate; one for each of said columns.

6. A camera device as in claim 5, wherein said timing circuit includes a timer for first sampling all reset levels in a specific column on first charge storage elements, and then for second sampling all signal levels on second charge storage elements.

7. A camera device as in claim 1, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout.

8. A camera device as in claim 7, wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated on said substrate.

9. A camera device as in claim 1, wherein said photoreceptors are photodiodes.

10. A camera device as in claim 1, wherein said photoreceptors are photogates.

11. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that a least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors.

12. A camera device as in claim 11, wherein said signal controlling device includes a column-parallel read out device, which reads out a row of said photoreceptors at substantially the same time.

13. A camera device as in claim 11, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout.

14. A camera device as in claim 13, wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated on said substrate.

15. A camera device as in claim 13, wherein said column selector includes presettable start and stop column decoder counters, which are preset to start and stop at any desired value.

16. A camera device as in claim 15, further comprising an input data bus, connected to the camera device, values on said data bus being used to preset said start and stop column decoder counters.

17. A camera device as in claim 11, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

18. A camera device as in claim 17, wherein said readout amplifier is preferably within and/ or associated with one element of the array.

19. A camera device as in claim 17, wherein said photoreceptors are photodiodes.

20. A camera device as in claim 17, wherein said photoreceptors are photogates.

21. A camera device as in claim 11, further comprising a mode selector device, selecting a mode of operation of said chip.

22. A camera device as in claim 21, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

23. A camera device as in claim 11, further comprising a correlated double sampling circuit.

24. A camera device as in claim 11, wherein said timing circuit controls readout from said chip in a correlated double sampling mode.

25. A camera device as in claim 22, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

26. A camera device as in claim 11, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

27. A camera device as in claim 11, further comprising fixed pattern noise reduction circuits, on said substrate.

28. A camera device as in claim 11, further comprising a double delta sampling element integrated on the chip, which shorts sampled signals during the readout cycle reducing column fixed pattern noise.

29. A camera device as in claim 11, further comprising a noise reduction circuit.

30. A camera device as in claim 11, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

31. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors.

32. A camera device as in claim 31, wherein said signal controlling device includes a column-parallel read out device, which reads out a row of said photoreceptors at substantially the same time.

33. A camera device as in claim 32, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout.

34. A camera device as in claim 31, further comprising an input data bus, connected to the camera device, values on said data bus being used to preset said start and stop values.

35. A camera device as in claim 31, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

36. A camera device as in claim 35, wherein said readout amplifier is preferably within and/ or associated with one element of the array.

37. A camera device as in claim 31, wherein said photoreceptors are photodiodes.

38. A camera device as in claim 31, wherein said photoreceptors are photogates.

39. A camera device as in claim 31, wherein said photoreceptors are either photogates or photodiodes, further comprising a mode selector device which selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

40. A camera device as in claim 31, further comprising a correlated double sampling circuit integrated on the chip.

41. A camera device as in claim 31, wherein said timing circuit controls readout from said chip in a correlated double sampling mode.

42. A camera device as in claim 39, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

43. A camera device as in claim 31, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

44. A camera device as in claim 31, further comprising a noise reduction circuit.

45. A camera device as in claim 44, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

46. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors in a first mode or in a second mode, depending on a type of photoreceptor being used.

47. A camera device as in claim 46, wherein said photoreceptor is one of a photodiode or a photogate, and said array is controlled into said first mode for said photogate and in said second mode for said photodiode.

48. A camera device as in claim 46, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

49. A camera device as in claim 48, wherein said readout amplifier is preferably within and/ or associated with one element of the array.

50. A camera device as in claim 47, further comprising a correlated double sampling circuit.

51. A camera device as in claim 47, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

52. A camera device as in claim 47, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

53. A camera device as in claim 46 further comprising a noise reduction circuit.

54. A camera device as in claim 52, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

55. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of

operation of said array of photoreceptors to read at least one element of the array by first reading a reset level of said at least one element, and subsequently, after an integration time, second reading a charged level of said at least one photoreceptor, said reading and said second reading producing output signals based on both said charged level and said reset level.

56. A single chip camera device as in claim 55 wherein an output signal is equal to said charged level minus said reset level.

57. A camera device as in claim 55, wherein said signal controlling device includes a column-parallel read out device, which reads out a column of said photoreceptors at substantially the same time.

58. A camera device as in claim 55, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

59. A camera device as in claim 58, wherein said readout amplifier is preferably within and/ or associated with one element of the array.

60. A camera device as in claim 58, wherein said photoreceptors are photodiodes.

61. A camera device as in claim 58, wherein said photoreceptors are photogates.

62. A camera device as in claim 55, further comprising a mode selector device, selecting a mode of operation of said chip.

63. A camera device as in claim 62, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

64. A camera device as in claim 63, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

65. A camera device as in claim 55, wherein said timing circuit allows changing an integration time for said array of photoreceptors by changing a time interval between said first and second reading.

66. A camera device as in claim 55, further comprising fixed pattern noise reduction circuits, on chip.

67. A camera device as in claim 55, further comprising a noise reduction circuit.

68. A camera device as in claim 67, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

69. A camera device as in claim 67, wherein said noise reduction circuit is a fixed pattern noise reduction circuit.

70. A camera device as in claim 67, wherein said noise reduction circuit is a column to column fixed pattern noise reduction circuit.

71. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors; and

a circuit, integrated on said substrate, which reduces a fixed pattern noise.

72. A camera device as in claim 71, wherein said signal controlling device includes a column-parallel read out device, which reads out a row of said photoreceptors at substantially the same time.

73. A camera device as in claim 71, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

74. A camera device as in claim 73, wherein said readout amplifier is preferably within and/or associated with one element of the array.

75. A camera device as in claim 73, wherein said photoreceptors are photodiodes.

76. A camera device as in claim 73 wherein said photoreceptors are photogates.

77. A camera device as in claim 71, further comprising a mode selector device, selecting a mode of operation of said chip.

78. A camera device as in claim 77, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

79. A camera device as in claim 71, wherein said timing circuit controls readout from said chip in a correlated double sampling mode.

80. A camera device as in claim 78, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

81. A camera device as in claim 71, wherein said circuit that reduces fixed pattern noise includes at least one charge storage device, sampling a level indicative of reset.

82. A camera device as in claim 71, wherein said circuit that reduces fixed pattern noise includes at least two charge storage devices, one controlled by said timing circuit to first sample a level indicative of reset, and another controlled by said timing circuit to second sample a level indicative of a charged device.

83. A camera device as in claim 82, further comprising a shorting element that shorts together said two charge storage devices prior to sampling said reset level.

84. A camera device as in claim 82, wherein said timing circuit allows changing an integration time for said array of photoreceptors by changing a time between said first sample and said second sample.

85. A camera device as in claim 85, wherein said timing circuit times an operation of said fixed pattern noise reduction circuit to occur during a time of the video signal which is not being displayed.

86. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors,

said control portion including common logic elements to control row and address decoders and delay counters.

87. A camera device as in claim 86, wherein said signal controlling device includes a column-parallel read out device, which reads out a column of said photoreceptors at substantially the same time.

88. A camera device as in claim 86, wherein said signal controlling device includes a column selector allowing selection of a desired row for read out, and a row selector which allows selection of a desired row for readout.

89. A camera device as in claim 88 wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated on said substrate.

90. A camera device as in claim 88, wherein said column selector includes presettable start and stop column decoder counters, which are preset to start and stop at any desired value.

91. A camera device as in claim 90, further comprising an input data bus, connected to the camera device, values on said data bus being used to preset said start and stop column decoder counters.

92. A camera device as in claim 86, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

93. A camera device as in claim 92, wherein said readout amplifier is preferably within and/ or associated with one element of the array.

94. A camera device as in claim 92, wherein said photoreceptors are photodiodes.

95. A camera device as in claim 92 wherein said photoreceptors are photogates.

96. A camera device as in claim 86, further comprising a mode selector device, selecting a mode of operation of said chip.

97. A camera device as in claim 96, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

98. A camera device as in claim 86, further comprising a correlated double sampling circuit.

99. A camera device as in claim 86, wherein said timing circuit controls readout from said chip in a correlated double sampling mode.

100. A camera device as in claim 97, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

101. A camera device as in claim 86, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

102. A camera device as in claim 87, further comprising a noise reduction circuits, on chip.

103. A camera device as in claim 102, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

104. A camera device as in claim 102, wherein said noise reduction circuit is a fixed pattern noise reduction circuit.

105. A camera device as in claim 102, wherein said noise reduction circuit is a column to column fixed pattern noise reduction circuit.

106. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors arranged in rows and columns;

a charge storage element, associated with each said column;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors;

said control portion including common logic elements to control all pixels on a selected row to sample said all pixels onto said charge storage elements substantially simultaneously.

107. A device as in claim 106, wherein said logic elements control said pixels to first sample a reset level of each said row, and then to sample a charged level of said charge storage elements to produce information indicating a correlated signal indicative of a difference therebetween.

108. A device as in claim 106, wherein said control portion includes a plurality of column selection p-channel transistors, respectively associated with each column, said transistors being turned on to sample a column.

109. A device as in claim 106, wherein there is one of said charge storage elements associated with each of said columns.

110. A device as in claim 106, wherein there are two of said charge storage elements associated with each of said columns.

111. A camera device as in claim 106, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

112. A camera device as in claim 111, wherein said readout amplifier is preferably within and/or associated with one element of the array.

113. A camera device as in claim 111, wherein said photoreceptors are photodiodes.

114. A camera device as in claim 111, wherein said photoreceptors are photogates.

115. A camera device as in claim 106, further comprising a mode selector device, selecting a mode of operation of said chip.

116. A camera device as in claim 106, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

117. A camera device as in claim 106, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

118. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors arranged in rows and columns;

a charge storage element, associated with each said column;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors;

said control portion including logic elements to control a double delta sampling, integrated on the chip, which shorts sampled signals during the readout cycle, thereby reducing column fixed pattern noise.

119. A camera device as in claim 118, wherein said signal controlling device includes a column-parallel read out device, which reads out a row of said photoreceptors at substantially the same time.

120. A camera device as in claim 120, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout.

121. A camera device as in claim 118, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

122. A camera device as in claim 121, wherein said readout amplifier is preferably within and/ or associated with one element of the array.

123. A camera device as in claim 121, wherein said photoreceptors are photodiodes.

124. A camera device as in claim 121, wherein said photoreceptors are photogates.

125. A camera device as in claim 118, further comprising a mode selector device, selecting a mode of operation of said chip.

126. A camera device as in claim 125, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

127. A camera device as in claim 118, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

128. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and control portion, both of which are formed using a logic family that is compatible with CMOS.

said image acquisition portion integrated in said substrate including an array of photoreceptors in rows and columns;

first and second charge storage elements, associated with each said column;

said control portion integrated in said substrate including a signal controlling device,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of

operation of said array of photoreceptors, controlling said photoreceptors to output their signals such that said first charge storage element receives the signal indicative of reset and said second charge storage element receives a signal indicative of a charged state;

said control portion including a shorting element, formed on said substrate which shorts between said first and second charge storage elements to reduce noise produced thereby.

129. A device as in claim 128, wherein said photoreceptors are controlled to read out an entire column of information at one time, wherein there are one of said first and second charge storage elements on said substrate for each element of said column, and wherein there is one of said shorting elements on said substrate for each of said columns.

130. A camera device as in claim 128, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

131. A camera device as in claim 130, wherein said readout amplifier is preferably within and/or associated with one element of the array.

132. A camera device as in claim 130, wherein said photoreceptors are photodiodes.

133. A camera device as in claim 130, wherein said photoreceptors are photogates.

134. A camera device as in claim 128, wherein said timing circuit allows changing an integration time for said array of photoreceptors with changing timings of said first and second charge storage elements.

135. A method of controlling a single chip camera, comprising:

integrating, on a single substrate, an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS, said image acquisition portion integrated in said substrate including an array of photoreceptors, and a signal controlling device, controlling said

photoreceptors and a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors;

determining a first mode of operation for said photoreceptors being photogates, and a second mode of operation for said photoreceptors being photodiodes;

using said on-chip timing and control circuit to control sequences for accessing rows in a specified order depending on said mode of operation, using a first sequence for said first mode of operation for photogates, and a second mode of operation for said second mode for photodiodes, a timing for said first mode being different than a timing for said second mode.

136. A method of controlling a single chip camera, comprising:

integrating, on a single substrate, an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS, said image acquisition portion integrated in said substrate including an array of photoreceptors with output nodes, and a signal controlling

device, controlling said photoreceptors and a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors;

resetting said output nodes;

sampling a reset value as a first sample;

allowing said photoreceptors to accumulate charge, after resetting said output nodes;

sampling said output nodes after accumulating said charge, producing output signals indicative of a difference between said reset value and said sampled value after accumulating said charge.

137. A method in claim 137 wherein said reset level is sampled during a blanking interval of the video signal.

138. A method of controlling a single chip camera, comprising:

integrating, on a single substrate, an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS, said image acquisition portion integrated in said substrate including an array of photoreceptors with output nodes, and a signal controlling device, controlling said photoreceptors and a timing circuit

integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and also integrating at least two charge storage elements on said substrate;

first, shorting together specified nodes of said two charge storage elements;

after said first shorting, sampling voltages on said charge storage elements, said voltages being related to one another.

139. A method as in claim 138, further comprising:

sampling a reset value as a first sample;

allowing said photoreceptors to accumulate charge, after resetting said output nodes;

sampling said output nodes after accumulating said charge, producing output signals indicative of a difference between said reset value and said sampled value after accumulating said charge.

140. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors and a noise reduction circuit;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors and controlling an operation of said noise reduction circuit to occur during a time when signals are not being read from said array of photodetectors.

CMOS ACTIVE PIXEL SENSOR TYPE IMAGING SYSTEM ON A CHIP

Abstract of the Disclosure

Single substrate device is formed to have an image acquisition device and a controller. The controller on the substrate controls the system operation.

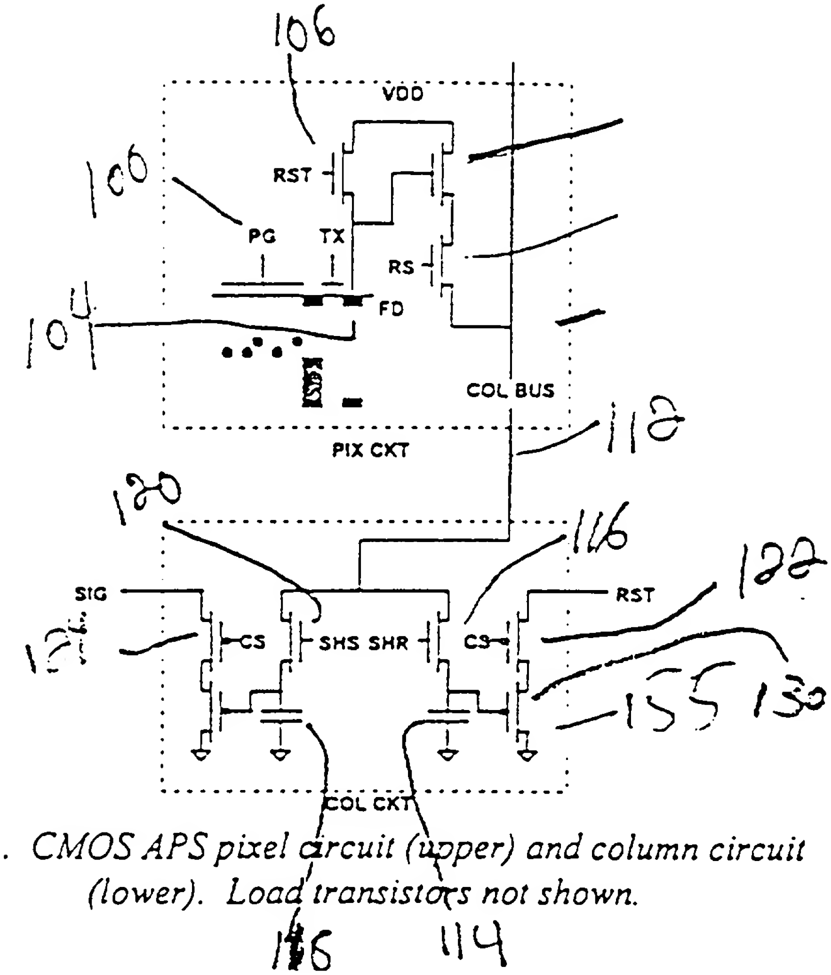


Fig. 1. CMOS APS pixel circuit (upper) and column circuit (lower). Load transistors not shown.

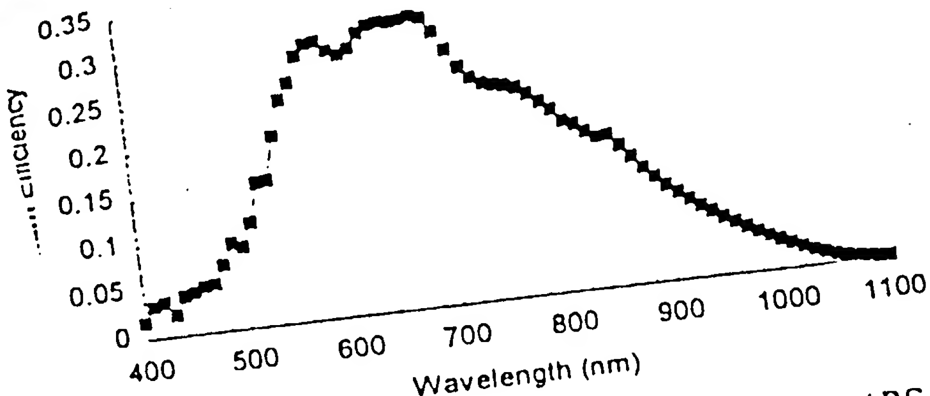


Fig 2. *Typical quantum efficiency of a CMOS APS pixel.*

On-Chip Timing and Control

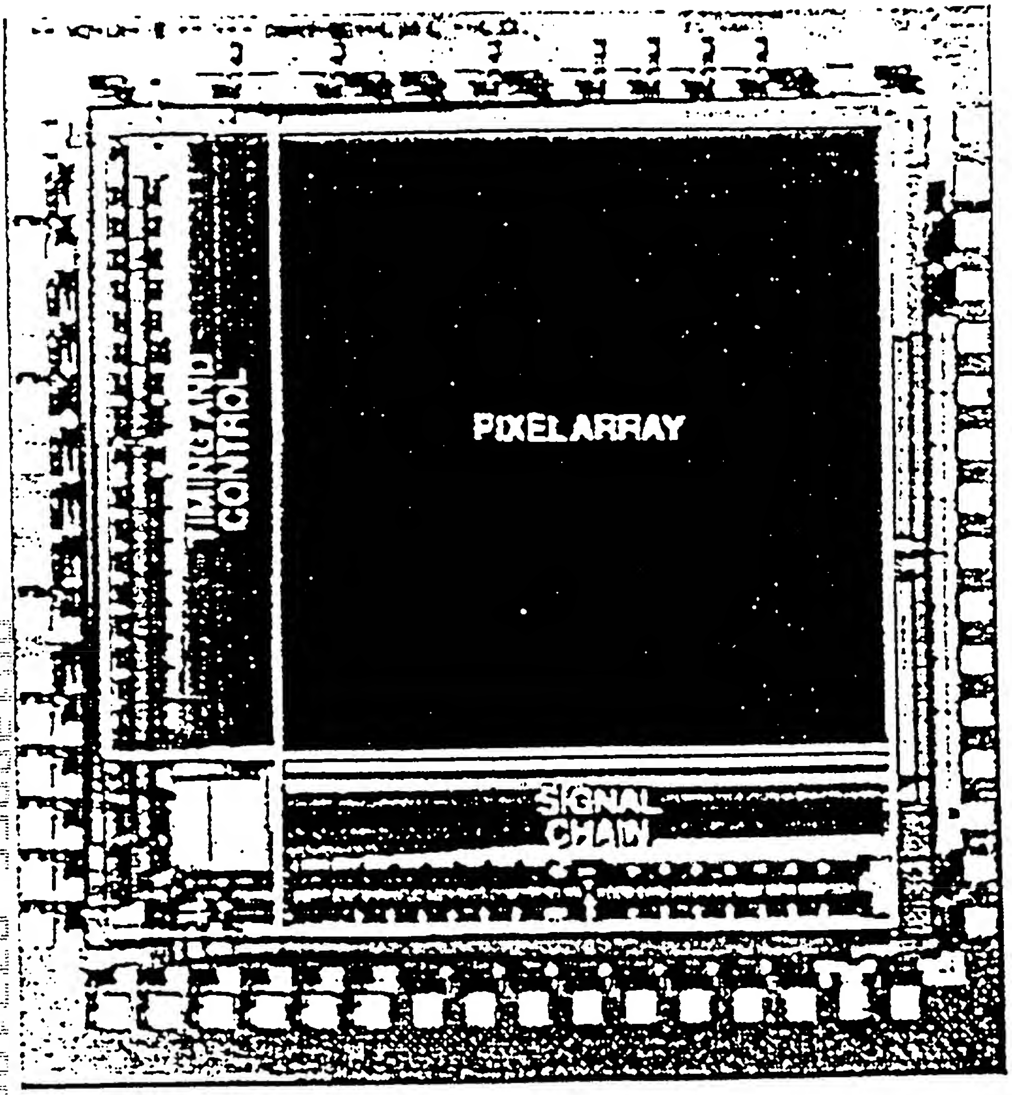


Fig. 7. Chip photograph of 128x128 element CMOS APS wit on-chip timing and control circuitry.

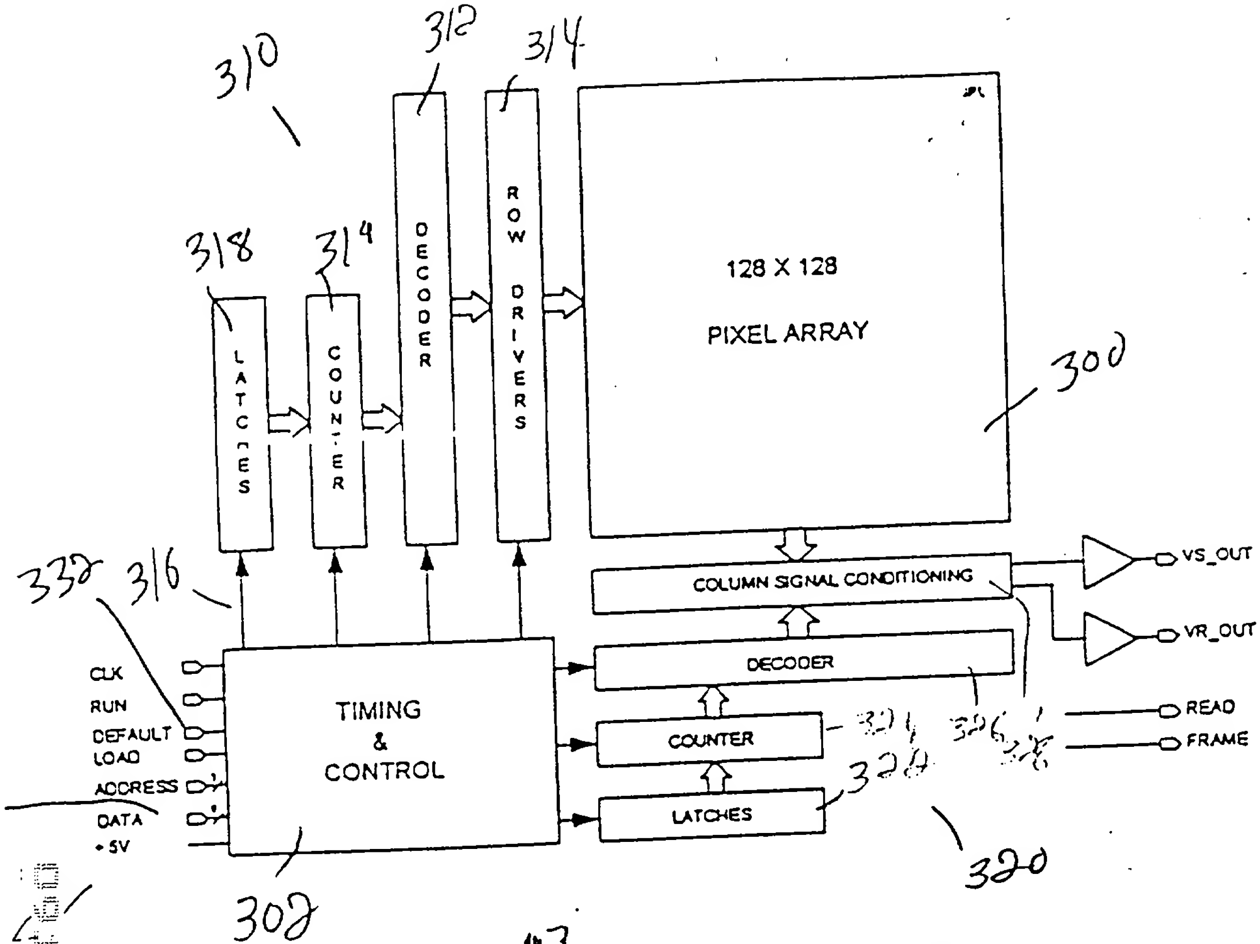


Figure 3. Block diagram of CMOS APS chip

08/ 2 7 5 5 0 7 2 1 0 0

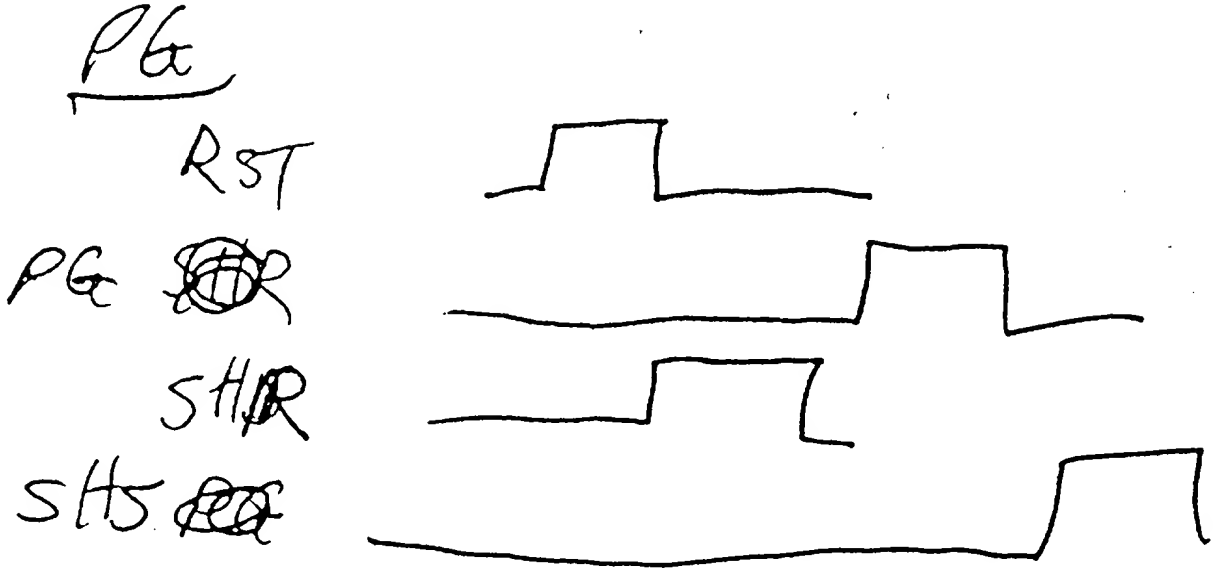


FIG 4A

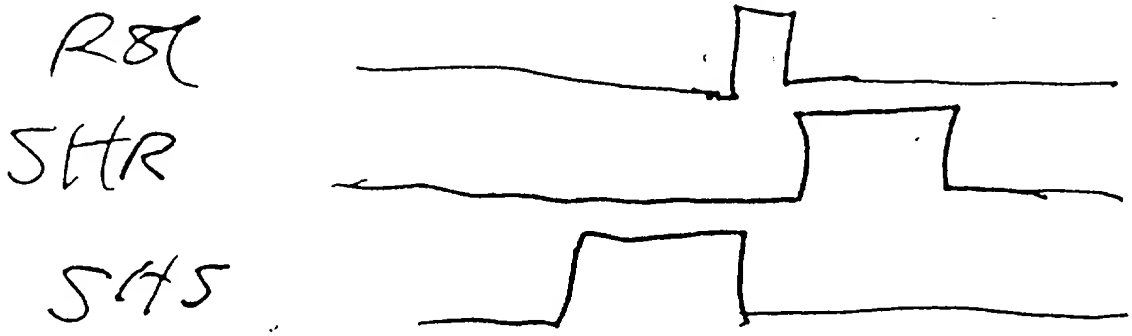


FIG 4B

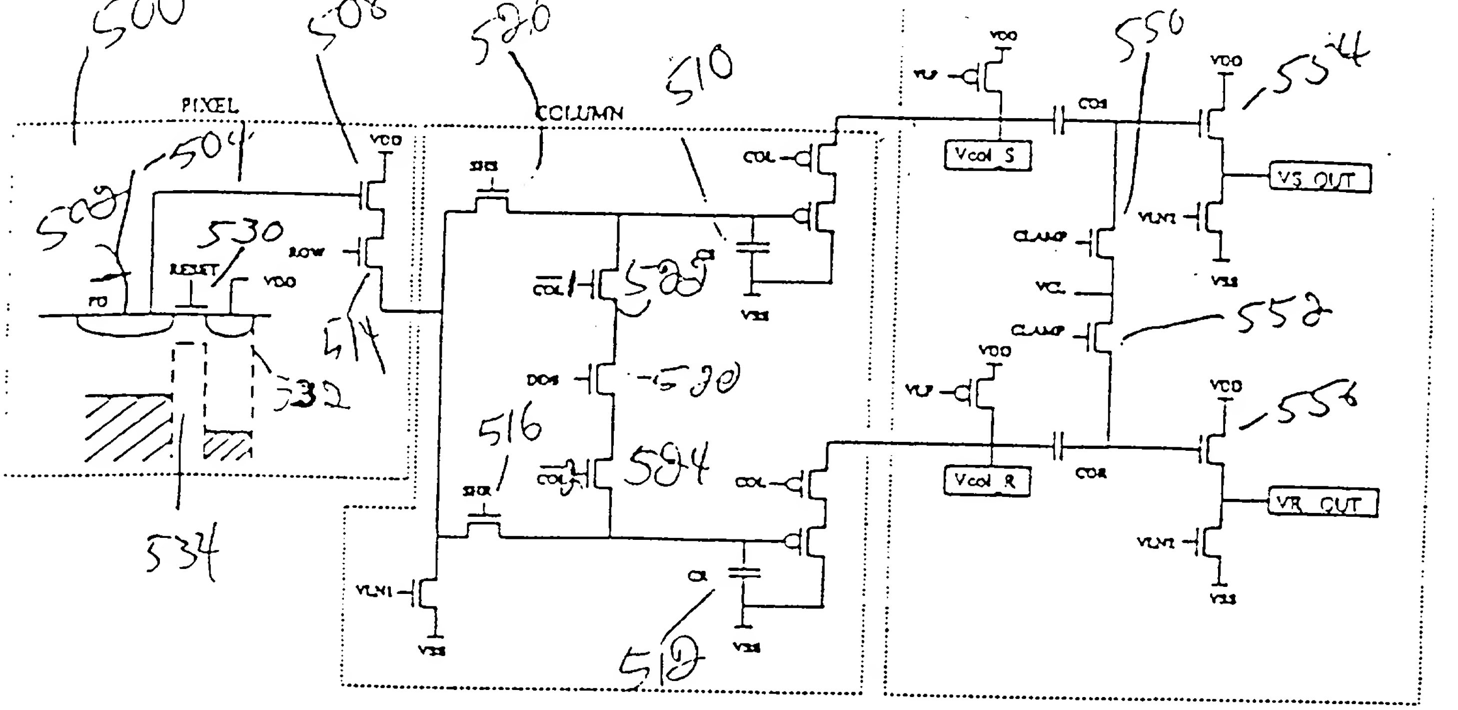


Figure 5. Schematic of active pixel sensor unit cell and readout circuitry

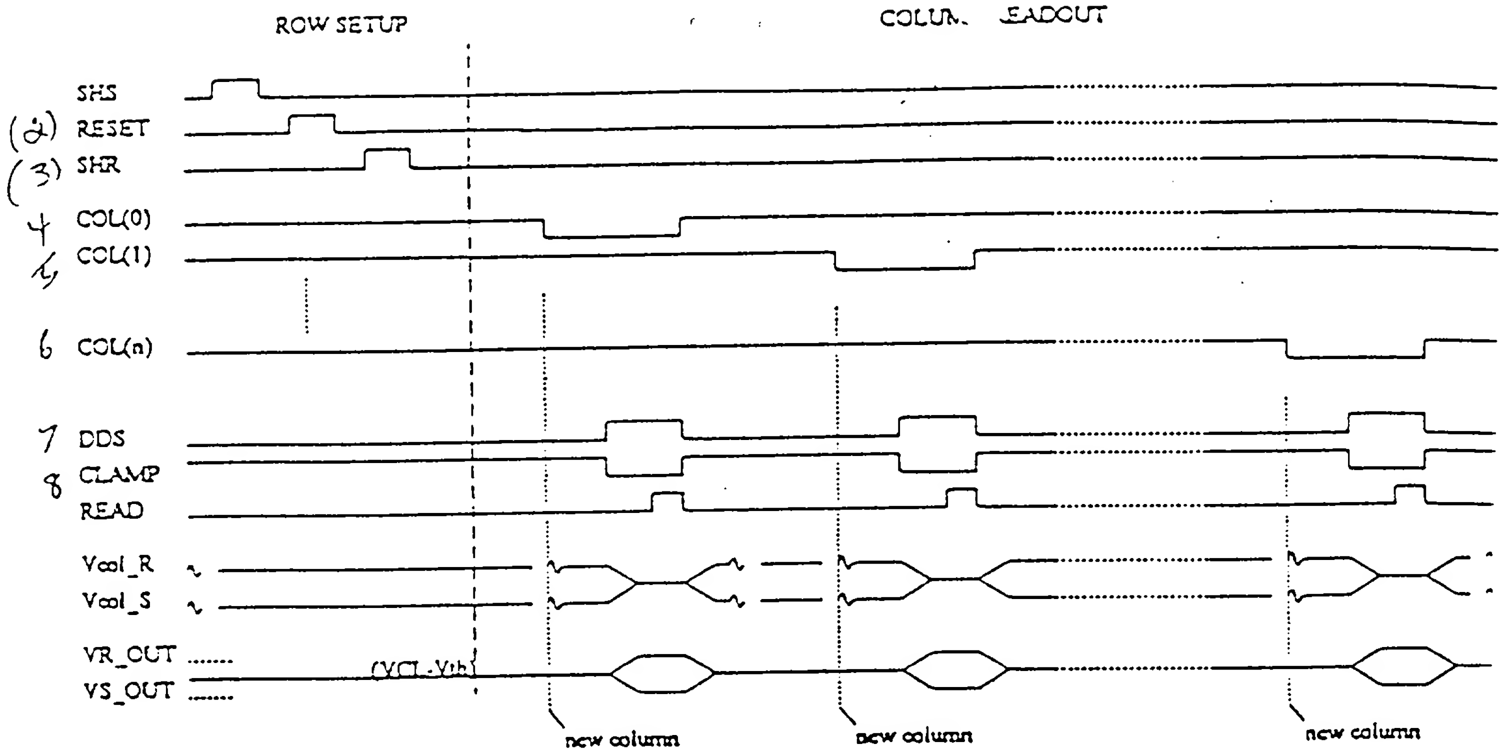


Figure 6. Timing diagram for setup and readout

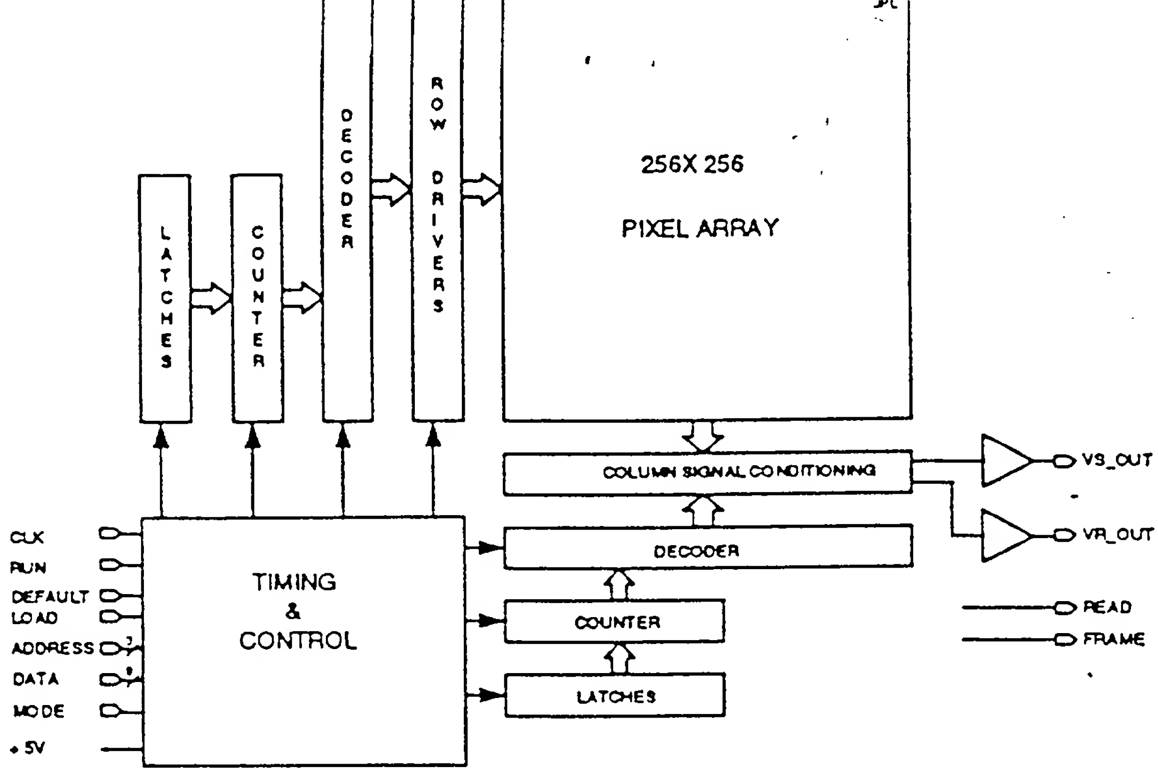
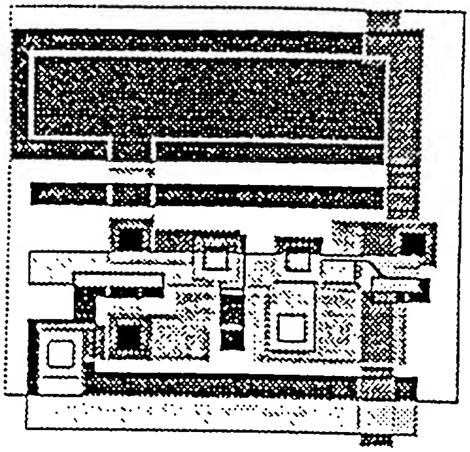


Fig 8

Figure Block diagram of CMOS APS chip



'ure 4. *Layout of pixel. Fill factor is 21%*

9

Array Size	256x256
Pixel Size	20.4 µm
Technology	1.2 µm n-well CMOS (HP)
Maximum Clock Rate	10 MHz
Minimum Clock Rate	none
Maximum Pixel Rate	2.5 MHz
Maximum Integration Delay	16 x 10^9 clock periods or 1600 secs at 10 MHz

PATENT
ATTORNEY DOCKET NO: 06816/019001

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled CMOS ACTIVE PIXEL SENSOR TYPE IMAGING SYSTEM ON A CHIP, the specification of which

☐ is attached hereto.
■ was filed on 1/24/97 as Application Serial No. 08/789,608 and was amended on .
☐ was described and claimed in PCT International Application No. ____________________
filed on ________________ and as amended under
PCT Article 19 on ________________.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information I know to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

U.S. SERIAL NO.	FILING DATE	STATUS
60/010,678	01/26/96	■ Pending ☐ Issued ☐ Abandoned
08/188,032	01/28/94	■ Pending ☐ Issued ☐ Abandoned

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Scott C. Harris, Reg. No. 32,030; William J. Egan, III, Reg. No. 28,411; David L. Feigenbaum, Reg. No. 30,378; John F. Land, Reg. No. 29,554; Ralph A. Mittelberger, Reg. No. 33,195; Hans R. Troesch, Reg. No. 36,950 and John R. Wetherell, Jr., Reg. No. 31,678.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

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Inventor's Signature: X [signature] Date: X 4-25-97

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COMBINED DEC RATION AND POWER OF ATTC EY CONTINUED

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